FREQUENCY SYNTHESIZING CIRCUIT

BACKGROUND OF THE INVENTION

1. Field of the invention

The present invention relates to a frequency synthesizing circuit, and particularly to
a frequency synthesizer which has a low frequency reference signal, a high frequency
output, and a high multiple for frequency synthesizing.

2. DESCRIPTION OF THE PRIOR ART

Phase-Locked Loop (PLL) is a technique usually used in a frequency synthesizing
circuit, as shown in Fig. 1. The basic framework thereof includes a phase-frequency
detector (PFD) 14, a charge pump loop filter (CPF) 16, a voltage control oscillator (VCO)
18 and a divider 20. Through the function of the PFD, the output frequency of the VCO
can be adjusted accordingly. When the loop is phase locked, the output frequency (f_{vco})
of the VCO and the frequency (f_{ref}) of the reference signal will satisfy the formula of f_{vco}
= N x f_{ref}, wherein N is a coefficient of the divider.

For an application of a high frequency generator (>100 MHz) with a low reference
frequency (<100 kHz), such as in a receiver of a video transmission system, a high
frequency clock generated from a screen horizontal synchronous signal (HSYNC) is
required for an analog to digital converter. In a traditional PLL, a high-ratio divider (N)
is required for frequency multiplication. But it often accumulates an extremely large
amount of phase errors. In addition, for a low frequency reference signal, the PLL loop
bandwidth should be narrowed down which may result in higher phase noise introduced
by VCO.

Thus it can be seen, the prior art described above still has some defects, is not a
good design, however, and is urgently to be improved.

Because of the technical defects of described above, the applicant keeps on carving unflaggingly to develop the frequency synthesizing circuit through wholehearted experience and research.

SUMMARY OF THE INVENTION

5   An object of the present invention is to provide a frequency synthesizing circuit which achieves double frequency multiplication by means of a phase-locked loop incorporated with a delay-locked loop so as to minimize phase error accumulations.

Another object of the present invention is to be applied in a programmable frequency synthesizer, especially for those have a low frequency reference signal (~kHz) 10   while to generate a high frequency output (>100MHz).

For achieving the purposes described above, the frequency synthesizer according to the present invention includes a frequency multiplier and a phase-locked loop, wherein the frequency multiplier converts a low frequency reference signal into a high frequency signal for being a reference signal to the phase-locked loop, so that the loop bandwidth of 15   the phase-locked loop can be increased to reduce output jitter.

Here, the frequency multiplier consists of a delayed locked loop and a phase synthesizer. The delay-locked loop is utilized to generate multi-phase output signals that equivalently divides a cycle of the reference signal. And the multiplication of reference signal is accomplished by synthesizing different output phases of the delay-locked loop, 20   which is controlled by the coefficient of the frequency multiplier. Through double frequency multiplication achieved by the delay-locked loop incorporated with the phase locked loop, the accumulated phase error can be reduced compared to that in a conventional phase-locked loop due to a wider loop bandwidth can be applied. Herein, frequency multiplied can be accomplished by adjusting the coefficients of frequency 25   multiplier or the divider of the phase-locked loop.

BRIEF DESCRIPTION OF THE DRAWINGS

The drawings disclose an illustrative embodiment of the present invention which serves to exemplify the various advantages and objects hereof, and are as follows:

Fig. 1 shows a framework of a conventional frequency synthesizer;

Fig. 2 shows a circuit diagram of a frequency synthesizing circuit according to the present invention;

Fig. 3 shows a diagram of a multiphase output signals that evenly divide a cycle;

Fig. 4 shows a circuit diagram generating a doubling frequency output, which is synthesized by four phases output signals that equivalently divides a cycle;

Fig. 5 shows a signal diagram generating a doubling frequency output, which is synthesized by four phases signals that equivalently divides a cycle;

Fig. 6 shows a signal diagram of a doubling frequency Q2 and a quadrupling frequency Q4, which are respectively synthesized by eight phases signals that equivalently divides a cycle;

Fig. 7 shows a framework of a $\frac{n}{2}$-multiplying phase synthesizer which is achieved by n phases signals that equivalently divides a cycle; and

Fig. 8 shows a framework of a programmable frequency synthesizing circuit.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Please refer to Fig. 2, which illustrates a frequency synthesizing circuit according to the present invention. The frequency synthesizing circuit mainly includes a frequency multiplier 43 and a phase-locked loop 42, wherein the frequency multiplier 43 converts a low frequency reference input signal f_{in} 62 into a high frequency output 65 for being provided as a reference to the phase-locked loop 42. A phase frequency detector (PFD) 58 compares the reference signal 65 with an output signal 67 to obtain phase and frequency difference and generates a modulated signal 68. Then, the modulated signal

68 is converted into a substantial DC voltage 69 by a loop filter 59 for further modulating a frequency of a voltage control oscillator 60.

An output signal 66 of the voltage controlled oscillator 60 can be downconverted by a divider 61, wherein the downconverted signal 67 outputted by a divider is connected to the phase frequency detector 58.

The frequency multiplier 43 according to the present invention includes a delay-locked loop and a phase synthesizer. The delay-locked loop is comprised of delay circuit 51-54, a phase detector (PD) 55 and a loop filter 56, wherein the delay circuit 51-54 is formed by "n" delay elements (herein the delay circuit is formed by the delay elements 51-54), the delay elements can be any circuit which can modulate the delay time, and the delay time is controlled by the control signal 63. An input of the reference signal 62 can be converted into signals with different phases and identical frequency to thereof at the output terminal of the delay circuit after passing through a series of delay elements. The phase detector 55 can detect the phase difference between an output phase 70 of the last delay element and the input reference signal 62 so as to generate a modulated signal 71. Then, the modulated signal 71 can control the delay time of the delay circuit through the control signal 63 which is converted into a substantial voltage by the loop filter 56. When the delay-locked loop is phase locked, a multiphase output signal at the delay circuit 51-54 can be obtained, wherein the multiphase output signal divides a cycle and makes an output phase of each delay element to have a phase difference of $\frac{2\pi}{n}$, as shown in Fig. 3.

Please refer to Fig. 4, which illustrates a basic framework of frequency doubling phase synthesizer. As shown in Fig. 4, $\varphi 1$, $\varphi 2$, $\varphi 3$ and $\varphi 4$ are four phases which evenly divide a cycle and are generated by the delay-locked loop, and the phase difference thereamong is:

$$\Delta \theta = 2\pi/4 = \pi/2$$

After a mix of the four phase signals, a frequency doubling signal can be obtained at the output terminals Q and Q'. A simple analysis is described as follows (please refer

to Fig. 5):

$$\varphi 1(\text{High}) = (0 \leqq \theta \leqq \pi) = (0 \leqq \theta \leqq \pi)$$

$$\varphi 2(\text{High}) = (\pi/2 \leqq \theta \leqq 3\pi/2) = (\Delta\theta \leqq \theta \leqq \pi + \Delta\theta)$$

$$\varphi 3(\text{High}) = (\pi \leqq \theta \leqq 2\pi) = (2\Delta\theta \leqq \theta \leqq \pi + 2\Delta\theta)$$

$$\varphi 4(\text{High}) = (3\pi/2 \leqq \theta \leqq 5\pi/2) = (3\Delta\theta \leqq \theta \leqq \pi + 3\Delta\theta)$$

$$Q(\text{High}) = (\Delta\theta \leqq \theta \leqq 2\Delta\theta) \cup (3\Delta\theta \leqq \theta \leqq 4\Delta\theta)$$

$$= (\pi/2 \leqq \theta \leqq \pi) \cup (3\pi/2 \leqq \theta \leqq 2\pi)$$

$$= \varphi 1 \times \varphi 2 + \varphi 3 \times \varphi 4$$

$$Q'(\text{High}) = (0 \leqq \theta \leqq \Delta\theta) \cup (2\Delta\theta \leqq \theta \leqq 3\Delta\theta)$$

$$= (0 \leqq \theta \leqq \pi/2) \cup (\pi \leqq \theta \leqq 3\pi/2)$$

$$= \varphi 1 \times \varphi 4 + \varphi 2 \times \varphi 3$$

A frequency doubler accomplished by phase synthesizing can be obtained to implement the Boolean function of Q and Q'.

According to this concept, through utilizing n phases output signals (n is even) which equivalently divide a cycle and have a phase difference of $\Delta\theta = \dfrac{2\pi}{n}$, an output result with a $\dfrac{n}{2}$- frequency multiplication can be obtained by a phase synthesizing. The general formula of the differential output is:

$$Q(\text{High}) = (\Delta\theta \leqq \theta \leqq 2\Delta\theta) \cup (3\Delta\theta \leqq \theta \leqq 4\Delta\theta) \cup$$

$$(\Delta 5\theta \leqq \theta \leqq 6\Delta\theta) \cup \ldots\ldots\ldots\ldots\ldots\ldots \cup$$

$$((n-1)\theta \leqq \theta \leqq n\Delta\theta)$$

$$= \varphi 1 \times \varphi 2 + \varphi 3 \times \varphi 4 + \varphi 5 \times \varphi 6 + \ldots\ldots + \varphi(n-1) \times \varphi n$$

$$Q'(\text{High}) = (0 \leqq \theta \leqq \Delta\theta) \cup (2\Delta\theta \leqq \theta \leqq 3\Delta\theta) \cup$$

$$(\Delta 5\theta \leqq \theta \leqq 6\Delta\theta) \cup \ldots\ldots\ldots\ldots\ldots\ldots \cup$$

$$((n-1)\theta \leqq \theta \leqq n\Delta\theta)$$

$$= \varphi n \times \varphi 1 + \varphi 2 \times \varphi 3 + \varphi 4 \times \varphi 5 + \circ \circ + \varphi(n-2) \times \varphi(n-1)$$

According to this formula, the frequency doubling concept can be extended. Assuming that it has n phases reference signals which divide a cycle (n= 2^M), through

synthesizing at different phases, different frequency multiplying output signals 2^{M-1}, 2^{M-2},..., 2^{1} can be generated.

Wherein a frequency 2^{M-1}-multiplying output signal has a general formula of:

Q (High) = $\varphi 1$x $\varphi 2 + \varphi 3$x $\varphi 4 + \varphi 5$x $\varphi 6 + ...+$ φ(n-1)x φn

- total 2^{M-1} items

Q' (High)= φnx $\varphi 1 + \varphi 2$x $\varphi 3 + \varphi 4$x $\varphi 5 + ...+$ φ(n-2)x φ(n-1)

-total 2^{M-1} items

A frequency 2^{M-2}-multiplying output signal has a general formula of:

Q (High) = $\varphi 1$x $\varphi 3 + \varphi 5$x $\varphi 7 + \varphi 9$x $\varphi 11 +$ ∘ ∘ $+$ φ(n-3)x φ(n-1)

-total 2^{M-2} items

Q' (High) = φ(n-1)x $\varphi 1 + \varphi 3$x $\varphi 5 + \varphi 7$x $\varphi 9 +$ ∘ ∘ $+ \varphi$(n-5)x φ(n-3)

-total 2^{M-2} items

A frequency $2^{1} = 2^{[M-(M-1)]}$ multiplying output signal has a general formula of:

Q (High) = $\varphi 1$x φ(1+M-1) $+ \varphi$(M+M-1) x φ(2M-1 + M-1)

-total 2^{1} items

Q' (High) = φ(n-M+2)x $\varphi 1 + \varphi$(1+ M-1) x φ(M+M-1)

-total 2^{1} items

Please refer to Fig. 6, which illustrates an output signal analyzing result of a doubling frequency Q2 and a quadrupling frequency Q4 which are synthesized by eight phases signals that equivalently divide a cycle.

Fig. 7 illustrates a framework of a $\frac{n}{2}$-multiplying phase synthesizer which is synthesized by n phases signals that equivalently divide a cycle.

Please refer to Fig. 8. A programmable frequency synthesizer includes a multi-phase generator 41, a phase selector 81, a multiplexer 82, a phase synthesizer 83 and a phase-locked loop 42, wherein the multi-phase generator 41 generates multiphase outputs that equivalently divide a cycle of a reference signal, which can be selectively outputted by the multiplexer 82 according to the phase selector 81. The phase synthesizer combines output phases from multiplexer so as to achieve frequency multiplication.

Moreover, the output of the phase synthesizer can be employed as a reference signal of the phase-locked loop 42. The phase selector 81 processes the phase addressing according to an external frequency multiplying control signal and then output a selected phase through the multiplexer. Take Fig. 6 as an example, an eight phases reference signal can respectively achieve a frequency doubling output and a frequency quadrupling output through synthesizing different phases.

The frequency synthesizing circuit according to the present invention, when being compared with the other prior arts, further includes the advantages as follows:

1. The present invention provides a frequency synthesizing circuit which utilizes double frequency multiplying functions by a phase-locked loop and a delay loop to mitigate phase error accumulation which may occur in the conventional phase-locked loop with only single frequency multiplying and narrow loop bandwidth.

2. The present invention provides a frequency synthesizing circuit which can be applied in any programmable frequency synthesizer. Furthermore, it can provide a good efficiency for being applied in a frequency synthesizer having a low frequency reference signal and a high frequency output.

While the present invention has been described in connection with what is considered the most practical and preferred embodiment, it is understood that this invention is not limited to the disclosed embodiment, but is intended to cover various arrangements included within the spirit and scope of the broadest interpretation so as to encompass all such modification and equivalent arrangements.